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IN THE CLAIMS:

Please amend claims 1, 2, and 5, and cancel claims 10-12 without prejudice

or disclaimer, as presented below.

1. (Currently Amended) A process of manufacturing a semiconductor

device comprising:

forming an insulating layer above a semiconductor layer;

forming a conductive layer including at least one of a tantalum layer and a

tantalum nitride layer, the conductive layer having a sidewall; and

etching the conductive layer by using a gas including SiCl₄ and NF₃,

wherein; a reactive material accumulates in the sidewall of the conductive layer to

function as protection and the ratio of the flow rate of the NF₃ to the flow rate of the

sum of the SiCl₄ and the NF ₃ is approximately 1 to approximately 30 % such that

an angle between the sidewall of the etched conductive layer and the insulating

layer is 85 to 90 degrees the conductive layer is etched to be substantially vertical.

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2. (Currently Amended) A process of manufacturing a semiconductor device

comprising:

forming an insulating layer above a semiconductor layer;

forming a conductive layer including at least one of a tantalum layer and a

tantalum nitride layer;

etching the conductive layer by using a gas including NF3 and C2F6 such

that approximately 70-80% of the tantalum layer and the tantalum nitride layer are

etched fluorocarbon; and

subsequently etching the conductive layer again by using a gas including

SiCl₄ and NF₃, wherein; the ratio of the flow rate of the NF₃ to the flow rate of the

sum of the SiCl₄ and the NF ₃ is approximately 1 to approximately 30 % such that

the conductive layer is etched to be approximately 89 degrees substantially vertical.

3. (Cancelled)

4. (Previously Presented) The process of manufacturing a semiconductor

device claimed in claim 1 wherein; the insulating layer includes at least one of

silicon oxide, silicon nitride and silicon oxynitride.

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5. (Currently Amended) A process of manufacturing a semiconductor device

comprising:

forming an insulating layer above a semiconductor layer;

forming a first tantalum nitride layer, body centered cubic lattice phase

tantalum layer and a second tantalum nitride layer in this order;

forming a gate electrode by etching the first tantalum nitride layer, the body

centered cubic lattice phase tantalum layer and the second tantalum nitride layer

with using a gas including SiCl₄ and NF₃; and

forming first and second impurity layers constituting a source region and a

drain region through introducing a impurity into the semiconductor layer, wherein;

the ratio of the flow rate of the NF3 to the flow rate of the sum of the SiCl4 and the

NF₃ is approximately 1 to approximately 30 % such that the conductive layer is

etched to be 90 degrees substantially vertical.

Claims 6-12. (Cancelled)

13. (Previously Presented) The process of manufacturing a semiconductor

device claimed in claim 2 wherein; the insulating layer includes at least one of

silicon oxide, silicon nitride and silicon oxynitride.

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